UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
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ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/819,883	LONG ET AL.
	Examiner	Art Unit
	Joseph Manoskey	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 March 2001_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-19_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-19_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _28 March 2001_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _2_.

4) ☐ Interview Summary (PTO-413) Paper No(s). _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Drawings

1.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5)

because they do not include the following reference sign(s) mentioned in the

description: Reference number "46' " from page 20, line 13. A proposed drawing

correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in

abeyance.

Specification

2.   The disclosure is objected to because of the following informalities:

3.   On page 6, line 19, reference number "42" is referred to as both a peripheral

device and a CD-ROM, but in Fig. 1 it is only referred to as a generic peripheral device.

The second "42" on line 19 of page 6 should be removed.

4.   On page 6, line 21, the CPU is referred by reference number "20" but in Fig. 1 it

is labeled by reference number "22". The second "20" on line 21 of page 6 should be

changed to "22".

5.   On page 8, line 6, the references "26" and "26' " are used to refer to the

redundant I/O systems. It is believed that these two references should be "26" " and

"26''' ".

6.   On page 30, line 19, the reference number "151" is used to refer to the switches

of Fig. 7. The reference number "151" on line 19 of page 30 should be changed to

"155".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by
another filed in the United States before the invention by the applicant for patent or (2) a patent
granted on an application for patent by another filed in the United States before the invention by the
applicant for patent, except that an international application filed under the treaty defined in section
351(a) shall have the effects for purposes of this subsection of an application filed in the United States
only if the international application designated the United States and was published under Article 21(2)
of such treaty in the English language.

8.   Claim 1, 2, 3, 5, 8, 11, 12, 14, 16, 17, and 19 are rejected under 35 U.S.C. 102(e)

as being anticipated by Starke et al., U.S. Patent 6,643,763, hereinafter referred to as

"Starke".

9.   Referring to claim 1, Starke discloses processing system that is comprised of a

plurality of processing elements executing identical instruction streams (See Fig. 1 and

9, and Col. 11, lines 43-47). Starke also discloses a target in communication with one

of the processing elements (See Col. 13, lines 40-41). Finally Starke discloses a

connecting fabric, which is interpreted as a switching fabric, communicating the

transactions between the processing elements and the target (See Fig. 9 and Col. 13,

lines 20-22).

10.   Referring to claim 2, Starke teaches the using synchronization when exiting

MIMD mode and entering a mode where the processors execute the same instruction

stream (See Col. 11, lines 4-7), this synchronization is interpreted as the processors

working in lock-step.

11.   Referring to claim 3, Starke discloses the processing elements being a CPU (See

Fig. 1 and 9).

12.   Referring to claim 5, Starke discloses the target being a processing element (See

Fig. 1 and 9, and Col. 13, lines 40-41).

13.   Referring to claim 8, Starke discloses the use of control scheme for the piping of

input and output data that is sent through the interconnect system, which is interpreted

as channel adapters (See Fig. 11 and 12, and Col. 15, lines 60-62).

14.   Referring to claims 11 and 12, Starke discloses a destination CPU ID for

addressing the processing elements (See Col. 13, lines 40-41), this is interpreted as a

respective device address or node address.

15.   Referring to claim 14, Starke teaches a plurality of processing elements

generating replicated execution to target addresses (See Col. 11, lines 43-47), this is

interpreted as identical transactions. Starke also teaches the use of a connecting fabric

for communicating the transactions (See Fig. 9, Col. 13, lines 20-22 and 43-47).

16.   Referring to claims 16 and 17, Starke discloses a destination CPU ID for

addressing the processing elements (See Col. 13, lines 40-41), this is interpreted as a

respective device address or node address.

17.   Referring to claims 19, Starke discloses the processors containing adapters,

which then transfer data to the switching fabric (See rejection of claim 8). The switching

fabric transfers the data to the target, in this case another processor, via the adapter

(See Fig. 1, 9, 11, 12, and Col. 13, lines 40-41 and Col. 15 60-62).

Claim Rejections - 35 USC § 103

18.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set
forth in section 102 of this title, if the differences between the subject matter sought to be patented and
the prior art are such that the subject matter as a whole would have been obvious at the time the
invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

19.   Claims 4, 6, 7, 13, and 18, rejected under 35 U.S.C. 103(a) as being

unpatentable over Starke in view of Thorson et al., U.S. Patent 6,643,764, hereinafter

will be referred to as "Thorson".

20.   Referring to claim 4, Starke teaches all the limitations (See rejection of claim 3)

except for the CPU being comprised of a plurality of processors, however Starke

discloses transferring data from processor to processor without passing through

memory (See Col. 2, lines 23-27). Thorson discloses a multiprocessor system

comprised of processor nodes connected via a router, which is interpreted as a

switching fabric, where each processor node is comprised of a plurality of processors

(See Fig.1). It would be obvious to one of ordinary skill in the art at the time of the

invention to use the processor nodes comprising of a plurality of processors of Thorson

for the processors of Starke. This would have been obvious to one of ordinary skill in

the art at the time of the invention to do because the infrastructure permits access to

data in the same manner as accessing local memory (See Thorson, Col. 1, lines 27-34).

21.   Referring to claim 6, Starke discloses all the limitations (See rejection of claim 1)

except for target being a peripheral component. Thorson teaches the ports of the router

being associated with I/O interface ports (See Col. 3, lines 49-52), which is interpreted

as including a peripheral component. It would have obvious to one of ordinary skill in

the art at the time of the invention to use the peripheral components of Thorson as the

target of Starke. This would have been obvious to one of ordinary skill in the art to do

because it provides the processor access to the peripheral components in the same

manner as memory.

22.   Referring to claim 7, Starke and Thorson teach all the limitations (See rejection of

claim 6) including the use of I/O interface ports (See Thorson, Col. 3, lines 49-52),

which are interpreted as channel adapters.

23.   Referring to claim 13, Starke discloses all the limitations (See rejection of claim

1) except Starke is silent on what format the data is passed through the switching fabric.

Thorson teaches the data being transmitted in the format of packets (See Col. 4, lines

1-2). It would be obvious to one of ordinary skill in the art at the time of the invention to

pass the data of Starke as the packets of Thorson. This would be obvious to one of

ordinary skill in the art at the time of the invention to do because the packet helps

determine the route taken to reach the destination (See Thorson, Col. 4, lines 1-11),

which helps control the flow of traffic and reduce bottlenecking.

24.   Referring to claim 18, Starke discloses all the limitations (See rejection of claim

14) except for target being a peripheral component. Thorson teaches the ports of the

router being associated with I/O interface ports (See Col. 3, lines 49-52), which is

interpreted as including a peripheral component. It would have obvious to one of

ordinary skill in the art at the time of the invention to use the peripheral components of

Thorson as the target of Starke. This would have been obvious to one of ordinary skill

in the art to do because it provides the processor access to the peripheral components

in the same manner as memory.

25.   Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Starke in view of Wardrop, U.S. Patent 5,903,717, hereinafter referred to as "Wardrop".

26.   Referring to Claim 9 and 15, Starke discloses all the limitations (See rejection of

claims 1 and 14 respectively) except for the apparatus further comprising and method

using voter delay buffers wherein each of the voter delay buffers are in communication

with one of the processing elements, however Starke does teach the processors

running in SISD mode with replicated execution (See Col. 11, lines 43-46). Wardrop

teaches a voter ASIC for comparing the outputs of a plurality of processors (See Fig. 3).

It would be obvious to one of ordinary skill in the art at the time of the invention to

combine the voter ASIC of Wardrop with the replicated execution of processors Starke.

This would be obvious to one of ordinary skill in the art at the time of the invention to do

because it provides significant operational advantages using commercially available

parts (See Wardrop, Col. 4, lines 52-55) that would help facilitate efficient transfer of

information (See Starke, Col. 2, lines 16-18).

27.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Starke in

view of Avery, U.S. Patent 6,622,193, hereinafter referred to as "Avery".

28.   Referring to claim 10, Starke teaches all the limitations (See rejection of claim 1)

except for a plurality of DMA in communication with the switching fabric. Avery

discloses using a DMA in communication with a switching fabric (See Col. 11, lines 3-5).

It would be obvious to one of ordinary skill in the art at the time of the invention to use

the DMA of Avery with the switched fabric of Starke. This would be obvious to one of ordinary skill in the art to do because it provides an autonomous method of accessing memory for processors (See Col. 2, lines 59-60).

Conclusion

29.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,226,152 to Klug et al.

U.S. Patent 6,141,770 to Fuchs et al.

U.S. Patent 6,289,022 to Gale et al.

U.S. Patent 6,636,933 to MacLellan et al.

U.S. Patent Application Pub. US 2001/0036181 to Rogers

U.S. Patent Application Pub. US 2002/0129296 to Kwiat et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JDM
December 18, 2003

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